What is claimed is:

CLAIMS

Sub a1

1. A shallow trench isolation structure in a substrate, said shallow trench isolation structure comprising:

a trench in said substrate; and

a nitride liner recessed within said trench, such that an uppermost surface of said nitride liner is disposed below a transistor channel depth, said transistor channel depth representing a width of a transistor disposed in a well beside said shallow trench isolation structure.

2. A shallow trench isolation structure in a substrate as recited in claim 1, wherein said transistor is a P-FET transistor.

3. A shallow trench isolation structure in a substrate as recited in claim 1, wherein the uppermost surface of said nitride liner is disposed greater than 1000 angstroms below a top surface of said substrate.

4. A shallow trench isolation structure in a substrate as recited in claim 1, further comprising:

an oxide layer disposed within the trench, said oxide layer underlying said nitride liner; and

an oxide fill disposed above said nitride liner such that the nitride liner is encapsulated by the oxide fill and oxide layer.

5. A shallow trench isolation structure in a substrate as recited in claim 4, wherein the oxide fill extends above said uppermost surface of said nitride liner, substantially to a top surface of said substrate, such that substantially no void exists above said uppermost surface of said nitride liner.

6. A shallow trench isolation structure in a substrate as recited in claim 2, further comprising:

an oxide fill disposed above said nitride liner such that said oxide fill extends above the uppermost surface of said nitride liner to substantially a top surface of said substrate, such that substantially no polysilicon material is disposed within the trench.

7. A shallow trench isolation structure in a substrate as recited in claim 6, wherein the oxide fill is tetraethylorthosilicate.

8. A shallow trench isolation structure in a substrate, said shallow trench isolation structure comprising:

a trench in the substrate;

a nitride liner disposed within said trench; and

an oxide fill disposed above said nitride liner, such that said oxide fill extends above an uppermost surface of said nitride liner substantially to a top surface of said substrate.

9. A shallow trench isolator in a substrate as recited in claim 8, wherein the nitride liner is recessed within said trench such that said uppermost surface of said nitride

liner is below a channel depth, said channel depth being respresentative of a width of a channel associated with a device disposed beside said trench.

10. A shallow trench isolator in a substrate as recited in claim 8, wherein said device is a P-FET transistor and said channel depth is about 1000 angstroms below a top surface of said substrate, such that said nitride liner may trap substantially no charge traversing said channel of said P-FET transistor.

11. A shallow trench isolator in a substrate as recited in claim 8, wherein the oxide fill is disposed above said nitride liner such that substantially no polysilicon material is disposed within the trench.

12. A method for reducing hot carrier reliability problems in an integrated circuit device on a substrate, said device including a transistor having a channel, said channel having a channel depth, and said device also including a shallow trench isolation structure having a trench formed within said substrate, an oxide layer disposed within said trench, a nitride liner disposed within said trench above said oxide layer, said method comprising:

depositing a layer of photoresist within said trench over said nitride liner;

etching said nitride liner to a first level, said first level being below said channel depth; and

removing said photoresist plug.

13. A method as recited in claim 12, further comprising:

depositing an oxide fill layer after said etching, such that said nitride liner is completely encapsulated between said oxide fill and said oxide layer.

14. A method as recited in claim 13, wherein the oxide fill layer is deposited above an uppermost surface of said nitride liner to substantially a top surface of said substrate.

15. A method as recited in claim 12, further comprising:

recessing said photoresist plug to a level deeper than said channel depth, said recessing being performed before said etching of said nitride liner.

16. A method as recited in claim 15, wherein said first level is substantially even with an upper surface of said photoresist plug after said recessing.

17. A method as recited in claim 13, wherein said deposition of said oxide fill is performed using a chemical vapor deposition process.

18. A method as recited in claim 15, wherein said recessing is performed using a downstream plasma etch process.

19. A method as recited in claim 12, wherein said etching is performed using an anisotropic etch process.

20. A method as recited in claim 19, wherein said anisotropic etch process is a plasma etch process.

21. A method for reducing hot carrier reliability problems in an integrated circuit device on a substrate, said device including a transistor having a channel, said channel having a channel depth, and said device also including a shallow trench

isolation structure having a trench formed within said substrate, an oxide layer disposed within said trench, a nitride liner disposed within said trench above said oxide layer, said method comprising:

depositing a photoresist plug within said trench over said nitride liner;

recessing said photoresist plug to a first level deeper than said channel depth;

etching said nitride liner to a second level, said second level being below said channel depth;

removing the recessed photoresist plug; and

depositing an oxide fill layer such that said nitride liner is completely encapsulated between said oxide fill and said oxide layer.

22. The method of claim 21 wherein said second level is substantially even with an upper surface of said photoresist plug after said recessing.

23. A method for reducing hot carrier reliability problems in an integrated circuit device on a substrate having a pad nitride layer overlying an oxide layer overlying an upper surface of said substrate, said device including a transistor having a channel, said channel having a channel depth, and said device also including a shallow trench isolation structure having a trench formed within said substrate, an oxide layer disposed within said trench, a nitride liner disposed within said trench above said oxide layer, said method comprising:

depositing a photoresist plug within said trench overlying said nitride liner;

etching said nitride liner to a level below said channel depth;

removing said photoresist plug;

depositing oxide fill within said trench above said nitride liner such that said nitride liner is encapsulated between said oxide layer and said oxide fill, and such that said oxide fill substantially completely fills said trench above an uppermost surface of said nitride liner;

removing said pad nitride layer overlying said upper surface of said substrate; and

depositing polysilicon over said shallow trench isolation structure, said deposition of the oxide fill being such that substantially no polysilicon is deposited within said trench.